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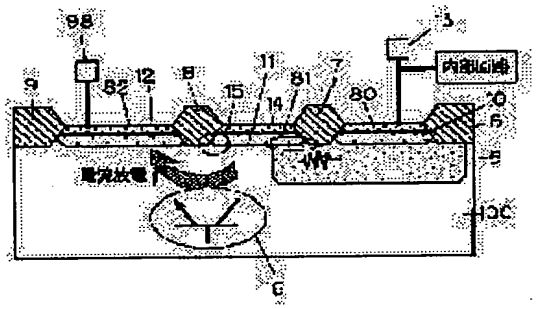
(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To improve an electrostatic breakdown voltage of an LSI utilizing a transistor having a low resistance source and drain.

SOLUTION: An N-type diffused region 10 is formed in such a wayas being surrounded by N well 5, while an N-type diffused region 11 is formed in such a way as being projected from N well 5 and is connected in direct to P type semiconductor substrate 100 in the vicinity of a silicon oxide film 8. Moreover, an N-type diffused region 12 is connected to a GND pad 98 and is isolated from the N-type diffused region 11 by means of a silicon oxide film 8. When a surge is applied thereto, the N well 5 becomes a resistance element. Therefore, the field at the junction area 15 between the N-type diffused region 11 and P-type semiconductor substrate 100 is alleviated and breakdown at this junction area 15 due to the discharging can be prevented.



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CLAIMS

[Claim(s)]
[Claim 1] The low concentration diffusion layer which has the 2nd conductivity type formed on the semi-conductor substrate which has the 1st conductivity type, The 1st high-concentration diffusion field which has the 2nd conductivity type which was formed on said low concentration diffusion layer, and was connected to the external electrode, The 2nd high-concentration diffusion field which has the 2nd conductivity type formed so that it might extend on said semi-conductor substrate from said low concentration diffusion layer, It is the semiconductor device which has the 3rd high-concentration diffusion field which has the 2nd conductivity type which was formed on said semi-conductor substrate and connected to the power-source electrode or the earth electrode. It is the semiconductor device characterized by for said 1st diffusion field and said 2nd diffusion field being separated by the 1st insulating layer, and said 2nd diffusion field and said 3rd diffusion field being separated by the 2nd insulating layer.
[Claim 2] The low concentration diffusion layer which has the 2nd conductivity type formed on the semi-conductor substrate which has the 1st conductivity type, The 1st high-concentration diffusion field which has the 2nd conductivity type which was formed on said low concentration diffusion layer, and was connected to the external electrode, The 2nd high-concentration diffusion field which has the 2nd conductivity type formed so that it might extend on said semi-conductor substrate from said low concentration diffusion layer, It is the semiconductor device which has the 3rd high-concentration diffusion field which has the 2nd conductivity type which was formed on said semi-conductor substrate and connected to the power-source electrode or the earth electrode. Said 1st diffusion field and said 2nd diffusion field are separated by the 1st insulating layer. Said 2nd diffusion field and said 3rd diffusion field are separated by said semi-conductor substrate. The gate electrode formed through gate dielectric film on said semi-conductor substrate which has separated said 2nd diffusion field and said 3rd diffusion field is formed. The semiconductor device characterized by forming an MOS transistor in said gate dielectric film, said gate electrode, said 2nd diffusion field, and said 3rd diffusion field.
[Claim 3] The 1st low concentration diffusion layer which has the 2nd conductivity type formed on the semi-conductor substrate which has the 1st conductivity type, The 1st high-concentration diffusion field which has the 2nd conductivity type which was formed on said 1st low concentration diffusion layer, and was connected to the external electrode, The 2nd high-concentration diffusion field which has the 2nd conductivity type formed so that it might extend on said semi-conductor substrate from said 1st low concentration diffusion layer, The 2nd low concentration diffusion layer which has the 2nd conductivity type formed on the semi-conductor substrate which has said 1st conductivity type, The 3rd high-concentration diffusion field which has the 2nd conductivity type which was formed on said 2nd low concentration diffusion layer, and was connected to the power-source electrode or the earth electrode, It is the semiconductor device which has the 4th high-concentration diffusion field which has the 2nd conductivity type formed so that it might extend on said semi-conductor substrate from said 2nd low concentration diffusion layer. It is the semiconductor device characterized by for said 1st diffusion field and said 2nd diffusion field being separated by the 1st insulating layer, for said 2nd diffusion field and said 4th diffusion field being separated by the 2nd insulating layer, and said 4th

diffusion field and said 3rd diffusion field being separated by the 3rd insulating layer.

[Claim 4] The 1st low concentration diffusion layer which has the 2nd conductivity type formed on the semi-conductor substrate which has the 1st conductivity type, The 1st high-concentration diffusion field which has the 2nd conductivity type which was formed on said 1st low concentration diffusion layer, and was connected to the external electrode, The 2nd high-concentration diffusion field which has the 2nd conductivity type formed so that it might extend on said semi-conductor substrate from said 1st low concentration diffusion layer, The 2nd low concentration diffusion layer which has the 2nd conductivity type formed on the semi-conductor substrate which has said 1st conductivity type, The 3rd high-concentration diffusion field which has the 2nd conductivity type which was formed on said 2nd low concentration diffusion layer, and was connected to the power-source electrode or the earth electrode, It is the semiconductor device which has the 4th high-concentration diffusion field which has the 2nd conductivity type formed so that it might extend on said semi-conductor substrate from said 2nd low concentration diffusion layer. Said 1st diffusion field and said 2nd diffusion field are separated by the 1st insulating layer. Said 2nd diffusion field and said 4th diffusion field are separated by the 2nd insulating layer. Said 4th diffusion field and said 3rd diffusion field are separated by the 3rd insulating layer. The gate electrode formed through gate dielectric film on said semi-conductor substrate which has separated said 2nd diffusion field and said 4th diffusion field is formed. The semiconductor device characterized by forming an MOS transistor in said gate dielectric film, said gate electrode, said 2nd diffusion field, and said 4th diffusion field.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the protection transistor and output transistor for the electrostatic-discharge prevention in semiconductor integrated circuit equipment.
[0002]
[Description of the Prior Art] In recent years, the cutback of parasitism resistance of a transistor is aimed at towards high integration of LSI, and improvement in the speed. The source of a transistor and the silicide-ized technique of a drain are mentioned as the typical technique. This reduces the source and drain resistance by silicide-izing the source and a drain diffusion field front face. Furthermore, since cutback-ization becomes easy about the source and drain area with this technique, high integration and improvement in the speed of LSI are realizable. However, low resistance-ization of the source and a drain brings about remarkable lowering of electrostatic-discharge pressure-proofing of LSI. This is because the field strength of a PN junction increases remarkably for the reduction in resistance of the source and a drain at the time of surge impression and the protection transistor itself carries out an electrostatic discharge in the protection transistor for preventing the electrostatic discharge of LSI.
[0003] Then, in order to prevent the above-mentioned destruction, the protection transistor of the conventionally following structures is proposed.
[0004] Drawing 9 shows the structure sectional view of the conventional protection transistor. Setting to drawing 9 , N well (for example, about three 1017-/cm) of low concentration [100 / 1 / a P-type semiconductor substrate and], the N type diffusion field of high concentration [4 / silicon oxide, and / 3 and 4 / 103 / 2 and] (for example, about three 1020-/cm), the titanium silicide film with which 101 and 102 were respectively formed on the N type diffusion field 3 and 4 front faces, the I/O pad with which 13 becomes an external electrode, and 98 are GND pads. On the P-type semiconductor substrate 100, the N type diffusion field 3 is formed so that it may be surrounded by the N well 1, and the N type diffusion field 4 is connected to the GND pad here.
[0005] The NPN lateral bipolar transistor 95 for electrostatic-discharge protection is formed of the above-mentioned configuration. That is, the base and the N type diffusion field 4 serve as [the N type diffusion field 3 and the N well 1 / the collector and the P-type semiconductor substrate 100] an emitter.
[0006] Although the protection transistor 95 turns on and the discharge current flows outside through a GND pad from the N type diffusion field 4 when the surge of + is impressed to the protection transistor constituted as mentioned above from the I/O pad 13, the N well 1 can serve as a resistance component, can ease the electric field between the N type diffusion field 3 and the P-type semiconductor substrate 100, and can prevent destruction.
[0007]
[Problem(s) to be Solved by the Invention] However, with the above configurations, in order to form the N well 1 and the N type diffusion field 4 using a separate mask, it had the trouble that had to extend the distance between both, i.e., the base width of face of a protection transistor, therefore a discharge rate fell, and destructive pressure-proofing of the internal circuitry of LSI fell as a result. Moreover, in

addition, since dispersion in the above-mentioned base width of face was large, it also had the trouble that the discharge property of the protection transistor 95 could not be made into homogeneity.
[0008] Even if this invention achieves low resistance-ization of the source of a transistor, and a drain in view of the above-mentioned trouble, it offers the protection transistor which can hold high electrostatic-discharge pressure-proofing.
[0009]
[Means for Solving the Problem] In order to solve the above-mentioned trouble the semiconductor device of this invention It has the 1st [of the 2nd path electrotyping formed on the semi-conductor substrate of the 1st path electrotyping], 2nd, and 3rd high-concentration diffusion fields, and the low-concentration diffusion layer of the 2nd path electrotyping. The 1st diffusion field is formed in a diffusion layer, and is connected to an external electrode, and the 2nd diffusion field is connected to a power-source electrode or an earth electrode. It is separated by the diffusion layer with the 1st diffusion field, and it connects electrically and the 3rd diffusion field has a diffusion layer, contact, and composition further separated by the semi-conductor substrate of the 2nd diffusion field and the 1st path electrotyping.
[0010] Moreover, the semiconductor device of this invention has the 1st of the 1st [of the 2nd path electrotyping formed on the semi-conductor substrate of the 1st path electrotyping], 2nd, 3rd, and 4th high-concentration diffusion fields, and the 2nd path electrotyping, and the 2nd low-concentration diffusion layer. The 1st diffusion field is formed in the 1st diffusion layer, and is connected to an external electrode. The 2nd diffusion field is formed in the 2nd diffusion layer, and is connected to a power-source electrode or an earth electrode. It is separated by the 1st diffusion layer with the 1st diffusion field, and the 3rd diffusion field is connected to the 1st diffusion layer, contact, and an electric target. It is separated by the 2nd diffusion layer with the 2nd diffusion field, and the 4th diffusion field has the 2nd diffusion layer, contact, and the composition that connected electrically and the 3rd and 4th diffusion field was further separated by the semi-conductor substrate of the 1st path electrotyping.
[0011]
[Function] By the above-mentioned configuration, by forming a resistance component in the bipolar protection transistor formed between high-concentration diffusion fields and its collector, or an emitter according to a low-concentration diffusion layer, this invention can form the base width of face of a protection transistor minutely, and can make dispersion in the discharge property small.
[0012]
[Example] The example of this invention is explained below, referring to a drawing.
[0013] (Example 1) The structure sectional view of the electrostatic-discharge protection transistor of an integrated circuit device [in / in drawing 1 / the 1st example of this invention] and drawing 2 show the top view in this example. Setting to drawing 1 , N well (for example, about three 1017-/cm) of low concentration [100 / 5 / a P-type semiconductor substrate and], the N type diffusion field of high concentration [12 / silicon oxide, and / 10, 11 and 12 / 9 / 6, 7, 8, and] (for example, about three 1020-/cm), the titanium silicide film with which 80, 81, and 82 were formed on the N type diffusion fields 10 and 11 and 12 front faces, the I/O pad with which 13 becomes an external electrode, and 98 are GND pads. The N type diffusion field 10 is formed so that it may be surrounded by the N well 5 on the P-type semiconductor substrate 100. Moreover, this N type diffusion field 10 is connected to the I/O pad 13. Moreover, this I/O pad 13 is connected with the internal circuitry of an integrated circuit device.
[0014] The N type diffusion field 11 is directly joined to the P-type semiconductor substrate 100 in the about eight-silicon oxide field 15, although it is formed in the form protruded from the N well 5 and has connected in the field 14 in the N well 5. Moreover, silicon oxide 7 dissociates in the N type diffusion field 10. The N type diffusion field 12 is separated by silicon oxide 8 in the N type diffusion field 11 while connecting with the GND pad 98. The NPN lateral bipolar transistor 16 for electrostatic-discharge protection is formed of the above-mentioned configuration. That is, the base and the N type diffusion field 12 serve as [the N type diffusion field 10, the N well 5, and the N type diffusion field 11 / the collector and the P-type semiconductor substrate 100] an emitter.

[0015] When the surge of + is impressed to such a protection transistor 16 of structure from the I/O pad 13 and it discharges to the GND pad 98, Although the discharge current flows into the N type diffusion field 11 through the N type diffusion field 10 and the N well 5, the protection transistor 16 turns on and it flows out of the N type diffusion field 12 through the P-type semiconductor substrate 100 Since the N well 5 between the N type diffusion field 10 and 11 serves as a resistance component even if the N type diffusion field 10 and 11 front faces are formed into titanium silicide and serve as low resistance at this time, The electric field for a joint 15 of the N type diffusion field 11 and the P-type semiconductor substrate 100 are eased, and destruction by part for this joint 15 by discharge can be prevented. Moreover, since the N type diffusion field 10 is surrounded by the N well 5, it does not produce junction destruction between the P-type semiconductor substrates 100. Furthermore, in this example, since separation width of face with the N type diffusion fields 11 and 12 turns into base width of face of the protection transistor 16, base width of face can be made detailed and, as a result, the improvement in an electrostatic-discharge proof pressure of the internal circuitry by improvement in the discharge rate of the protection transistor 16 is aimed at. Moreover, since dimension control is easy for the separation between diffusion fields, it can make the discharge property of the protection transistor 16 homogeneity.

[0016] (Example 2) The structure sectional view of the electrostatic-discharge protection transistor of an integrated circuit device [in / in drawing 3 / the 2nd example of this invention] and drawing 4 show the top view. The N type diffusion fields 24 and 25 and the N well 20 have the same composition as drawing 1 and the N type diffusion fields 10 and 11 of drawing 2 , and the N well 5.

[0017] In drawing 3 , the MOS transistor is formed with the high-concentration N type diffusion fields 25 and 26 and the high-concentration gate electrode 27, and the N type diffusion field 25 is formed in the form protruded from the N well 20, and is directly joined to the P-type semiconductor substrate 100 in the about 27 gate electrode field. When the surge of + is impressed to the I/O pad 13 and it discharges to the GND pad 98 in such a configuration, The discharge current flows into the N type diffusion field 25 through the N type diffusion field 24 and the N well 20. Furthermore, although the parasitism NPN lateral bipolar transistor 94 formed from the N type diffusion fields 25 and 26 and the P-type semiconductor substrate 100 turns on and it flows out of the N type diffusion field 26 into the exterior through the P-type semiconductor substrate 100 Since the N type diffusion field 24 and the N well 20 between 25 serve as a resistance component even if the N type diffusion field 25 and 26 front faces are formed into titanium silicide and serve as low resistance like the 1st example of the above, The electric field for a joint 32 of the N type diffusion field 25 and the P-type semiconductor substrate 100 are eased, and destruction by part for this joint 32 by discharge can be prevented. And the output transistor of high electrostatic-discharge pressure-proofing is real appearance **** by using the MOS transistor of the above-mentioned configuration as an output transistor which transmits the signal from the interior of an integrated circuit device to the exterior.

[0018] In addition, although the N type diffusion fields 12 and 26 of the 1st and 2nd above-mentioned examples are connected to the GND pad, respectively, it cannot be overemphasized that these may be connected to a power-source pad.

[0019] (Example 3) The structure sectional view of the electrostatic-discharge protection transistor of an integrated circuit device [in / in drawing 5 / the 3rd example of this invention] and drawing 6 show the top view. N well of low concentration [34 / a P-type semiconductor substrate, and / 33 and 34 / set to drawing 5 and / 100] (for example, about three 1017-/cm), The N type diffusion field of high concentration [42 / silicon oxide, and / 39, 40, 41 and 42 / 39 / 35, 36, 37, 38, and] (for example, about three 1020-/cm), The titanium silicide film with which 86, 87, 88, and 89 were formed on the N type diffusion fields 39, 40, and 41 and 42 front faces, the I/O pad with which 13 becomes an external electrode, and 99 are power-source pads. The N type diffusion fields 39 and 40 and the N well 33 have the same composition as the N type diffusion fields 10 and 11 of drawing 1 , and the N well 5. Furthermore, in this example, the N type diffusion field 42 is formed so that it may be surrounded by the N well 34 on the P-type semiconductor substrate 100. Moreover, this N type diffusion field 42 is

connected to the power-source pad 99. The N type diffusion field 41 is directly joined to the P-type semiconductor substrate 100 in the about 37-silicon oxide field, although it is formed in the form protruded from the N well 34 and has connected in the field 46 in the N well 34. Moreover, the N type diffusion fields 40 and 41 are separated by silicon oxide 37.

[0020] The NPN lateral bipolar transistor 43 for electrostatic-discharge protection is formed of the above-mentioned configuration. That is, the base, the N type diffusion field 41, the N well 34, and the N type diffusion field 42 serve as [the N type diffusion field 39 the N well 33, and the N type diffusion field 40 / the collector and the P-type semiconductor substrate 100] an emitter.

[0021] Since the N type diffusion field 39 and the N well 33 between 40 serve as a resistance component like the 1st example when the surge of + is impressed to such a protection transistor 43 of structure from the I/O pad 13 and it discharges to the power-source pad 99, the electric field for a joint 44 of the N type diffusion field 40 and the P-type semiconductor substrate 100 are eased, and destruction by part for this joint 44 by discharge can be prevented. Furthermore, in this example, since the N type diffusion field 41 and the N well 34 between 42 serve as a resistance component similarly when the surge of + is impressed from the power-source pad 99 and it discharges to the I/O pad 13, the electric field for a joint 45 of the N type diffusion field 41 and the P-type semiconductor substrate 100 are eased, and destruction by part for this joint 45 by discharge can be prevented. Moreover, since separation width of face with the N type diffusion fields 40 and 41 turns into base width of face of the protection transistor 43, base width of face can be made detailed and, as a result, improvement in an electrostatic-discharge proof pressure of the internal circuitry by improvement in the discharge rate of the protection transistor 43 is achieved.

[0022] (Example 4) The structure sectional view of the electrostatic-discharge protection transistor of an integrated circuit device [in / in drawing 7 / the 4th example of this invention] and drawing 8 show the top view. Although the 4th example has the almost same structure as the 3rd example, in the 3rd example, it differs by the 4th example to the N type diffusion fields 40 and 41 being separated by silicon oxide 37 in that the MOS transistor is formed with the N type diffusion fields 59 and 60 and a gate electrode.

[0023] When the surge of + is impressed to the I/O pad 13 and it discharges to the power-source pad 99 in such a configuration, Or since the N type diffusion field 58 and the N well 52 between 59 serve as a resistance component like the 3rd example when the surge of + is impressed from the power-source pad 99 and it discharges to the I/O pad 13, Or since the N type diffusion field 60 and the N well 53 between 61 serve as a resistance component, the electric field for a joint 65 of the part for a joint 96, the N type diffusion field 60, and the P-type semiconductor substrate 100 of the N type diffusion field 59 and the P-type semiconductor substrate 100 are eased, and destruction by part for these joints can be prevented. And the output transistor of high electrostatic-discharge pressure-proofing is realizable by using the MOS transistor of the above-mentioned configuration as an output transistor which transmits the signal from the interior of an integrated circuit device to the exterior.

[0024] In addition, these may be connected to the GND pad although the N type diffusion fields 42 and 61 of the 3rd and 4th above-mentioned examples are connected to the power-source pad, respectively.

[0025] Moreover, although the parasitism bipolar transistor of NPN is formed by each in the 1st, 2nd, 3rd, and 4th examples, the parasitism bipolar transistor may be formed by PNP.

[0026] Although the titanium silicide film is furthermore formed in the N type diffusion field front face of the 1st, 2nd, 3rd, and 4th examples, whether other silicide film, such as cobalt silicide film, is formed, for example or the metal membrane has accumulated, the same effectiveness is acquired to the improvement in an electrostatic-discharge proof pressure.

[0027]

[Effect of the Invention] This invention as mentioned above by forming a resistance component in the bipolar protection transistor formed between the separated high-concentration diffusion fields and its collector, or an emitter according to a low-concentration diffusion layer Since the electric field for a joint of a high-concentration diffusion field and a semi-conductor substrate are eased and destruction

for this joint by surge discharge can make detailed prevention **** and base width of face of a protection transistor at the time of surge impression The improvement in an electrostatic-discharge proof pressure of the internal circuitry by improvement in the discharge rate of the protection transistor is aimed at. Moreover, since dimension control is easy for the separation between high concentration diffusion fields, it can make the discharge property of a protection transistor homogeneity.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The structure sectional view of the electrostatic-discharge protection transistor in the 1st example of this invention
[Drawing 2] The top view of the electrostatic-discharge protection transistor in the 1st example of this invention
[Drawing 3] The structure sectional view of the ********** m ** transistor in the 2nd example of this invention
[Drawing 4] The top view of the electrostatic-discharge protection transistor in the 2nd example of this invention
[Drawing 5] The structure sectional view of the electrostatic-discharge protection transistor in the 3rd example of this invention
[Drawing 6] The top view of the electrostatic-discharge protection transistor in the 3rd example of this invention
[Drawing 7] The structure sectional view of the electrostatic-discharge protection transistor in the 4th example of this invention
[Drawing 8] The top view of the electrostatic-discharge protection transistor in the 4th example of this invention
[Drawing 9] The structure sectional view of the conventional electrostatic-discharge protection transistor
[Description of Notations]
1, 5, 20 N well
2, 6, 7, 8, 9 Silicon oxide
3, 4, 10, 11, 12 N type diffusion field
13 I/O Pad
14 N Type Diffusion Field and Connection Field of N Well
15 A Part for Joint of N Type Diffusion Field and P-type Semiconductor Substrate
16 NPN Parasitism Lateral Bipolar Transistor
17 18 Contact part between an N type diffusion field and metal wiring
19 20 Metal wiring
27 Gate Electrode
80, 81, 82 Titanium silicide film
98 GND Pad
99 Power-Source Pad
100 P-type Semiconductor Substrate

[Translation done.]